A Two Day National Symposium on Heterogeneous Computing: Platforms, Tools and Applications, August 31 and September 1, 2012

Program Schedule

DAY 1 (FRIDAY, AUGUST 31)

8:30-10:00 REGISTRATION
10:00-11:00 INAUGURAL SESSION

10:00-10:10 Lighting of the Lamp by Dignitaries
10:10-10:15 Invocation
10:15-10:20 Welcome Address by Prof S Sameen Fatima, Head, Dept. of CSE, UCE
10:20-10:25 "About the Symposium" by Prof S Ramachandram, Vice-Principal, UCE
10:25-10:30 Address by Prof VSS Kumar, Principal, UCE
10:30-10:45 Address by Guest of Honour, Mr Manoher Bommena, Senior Director & Site Leader, AMD Hyderabad
10:45-10:55 Address by Chief Guest, Prof Rameshwar Rao, VC, JNTU-H
10:55-11:00 Vote of Thanks by Mrs K Shyamala, Workshop Coordinator, CSE Dept., UCE

11:00-11:15 TEA BREAK

11:15-11:55 A NEW ERA OF COMPUTING
Mr Manoher Bommena, Senior Director, AMD

Diminishing returns in the single-core and multi-core arena led AMD to be at the forefront of the fusion innovation, creating what we today call the Accelerated Processing Unit (APU). This talk describes the journey to the AMD APU & beyond.

11:55-12:35 PROGRAMMING IN A HETEROGENEOUS WORLD
Dr K Srinidhi, Director, Product Application Engineering, AMD

One size does not fit all. In today's world of diverse applications and platforms, it is important to find the right tool for the right job. Heterogeneous computing addresses this limitation and opens the platform to drive developer innovation. This talk focuses on the challenges and opportunity with regards to programming on heterogeneous platforms.

12:35-1:15 FELICITATION FUNCTION

12:35-12:40 Welcome Address by Dr P Chandrasekhar, Head, Dept. of ECE, UCE
12:40-12:50 Address by Chief Guest, Prof S Satyanarayana, VC, OU
12:50-1:00 Felicitation of Prof Rameshwar Rao by HOD & Staff, ECE Dept., UCE
1:00-1:10 Address by Guest of Honour, Prof Rameshwar Rao, VC, JNTU-H
1:10-1:15 Vote of Thanks by Mr B Rajendra Naik, Workshop Coordinator, ECE Dept., UCE

1:15 -2:00 LUNCH (SERVED)

2:00 -3:15 OVERVIEW OF OPEN COMPUTING LANGUAGE (OpenCL)
Dr P Chandrasekhar & Prof S Ramachandram, UCE

OpenCL is a framework for writing programs that execute across heterogeneous platforms consisting of central processing unit (CPU), graphics processing unit (GPU), and other processors. OpenCL includes a language for writing kernels (functions that execute on OpenCL devices), plus application programming interfaces (APIs) that are used to define and then control the platforms. OpenCL provides parallel computing using task-based and data-based parallelism. The lecture will be followed by demonstration of example applications.

3:15–3:35 TEA BREAK

3:35-5:15 PARALLEL PROGRAMMING W/ OpenCL AND AMD APP SDK TOOLS
Mr Sushant Kumar & Mr Srinivasulu Charupally, AMD

This talk is on AMD APP Software Development Kit (SDK). AMD APP SDK is a complete development platform created by AMD to allow you to quickly and easily develop applications accelerated by AMD APP technology. The SDK allows you to develop your applications in a high-level language, OpenCL™ (Open Computing Language)

DAY 2 (SATURDAY, SEPTEMBER 1)

9:00– 10:00 HETEROGENEOUS COMPUTING PLATFORMS USED IN SATELLITE DATA PROCESSING TO ACHIEVE HIGH PERFORMANCE
Dr K Pramod Kumar, Scientist & Division Head HPC, Dept. of Space, ADRIN, India

This talk briefly describes issues and complexities involved in Satellite data processing and use of heterogeneous platforms– FPGAs, GP/GPUs and multicore CPUs for overcoming the data exodus and also achieving High Performance. Use of Open Standards minimize many of the issues such as- hardware and software integration, programming complexity, debugging and maintenance but also pose some other challenges.

10:00- 10:55 RECONFIGURABLE COMPUTING PLATFORM FOR EMBEDDED SYSTEMS
Mr K Ananda Babu, Scientist E, ANURAG, DRDO, India

This talk describes FPGA based reconfigurable systems that can be used for Embedded Processing in High-end applications like Multi-mode Multi-Service Radio, Stereoscopic Visualization and Pattern Recognition. These applications demand more computational power, higher logic functionality, and stringent timing behavior. Benefits of run-time re-configurability for performance are discussed.

10:55–11:15 TEA BREAK

11:15-12:15 EFFICIENT HARDWARE SOFTWARE PARTITIONING USING ADI DSP
Mr Rajesh Mahapatra, Senior Engineering Manager, Analog Devices

The complexity that a Digital Signal Processor handles today is huge. Increasing core complexity or speed is not the only solution. Efficient partitioning of work load between hardware and software is one elegant way of solving this problem. ADI's latest Blackfin DSP solves some of the MIPS hungry algorithms that is typical in imaging and video processing in a very elegant manner. These approaches are discussed in addition to a brief introduction of the architecture of the new Blackfin DSPs from Analog Devices.

12:15- 1:15 OPEN SOURCE SOLUTIONS FOR THE ZYNQ– ALL PROGRAMMABLE SOC
Prushothaman Palanichamy, Senior Product Marketing Engineer, Xilinx

The Zynq-7000 family combines an ARM® dual-core Cortex™-A9 MPCore™ processing system with programmable logic on a single chip. This architecture allows the device to boot like a processor and load custom hardware or accelerators when the CPU is running. This class of All Programmable device gives designers increased flexibility, performance and BOM cost reduction. But there are challenges in programming these new class of Heterogeneous Systems. This session focuses on listing the various challenges from Hardware-Software partitioning to addressing these challenges to design an optimized system by leveraging open source or industry standard tools and framework.

1:15-2:00 LUNCH (SERVED)

2:00–2:50 GROWTH IN COMPUTING PERFORMANCE
Prof R Govindarajulu, IIIT-H

This talk deals with the developments in hardware and software technologies and the challenges to be addressed with regard to power consumption, user productivity and performance. Future growth in computing must come from parallelism- multicore processors, must use a parallel programming model. Much software is written according to sequential programming model cannot easily be speeded up by using parallel processors. Rethinking programming models is needed so that programmers can express application parallelism naturally.

2:50-3:35 Aparapi FOR Java DEVELOPERS
Dr Prakash Raghavendra, Principal Member of Technical Staff, AMD

This talk focuses on Aparapi. An API for expressing data parallel workloads in Java and a runtime component capable of converting the Java byte code of compatible workloads into OpenCL™ so that it can be executed on a variety of GPU devices.

3:35-4:15 C++ AMP FOR C++ DEVELOPERS
Mr LK Suresh Kumar & Mrs K Shyamala, UCE

This talk presents the code-driven introduction on C++ Accelerated Massive Parallelism (C++ AMP) that helps C++ developers to understand how the performance can be improved by using parallelism on heterogeneous computing in a hardware-portable manner.

4:15– 5:15 VALEDICTORY SESSION

4:15-4:20 Opening remarks by Dr Chandrasekhar Head, Dept. of ECE, UCE, OU
4:20-4:30 Report on Symposium by Dr P Laxmina rayana, Senior Scientist, NERTU, OU
4:30-4:40 Address by Prof P Premchand, Dean, Faculty of Engineering, UCE, OU
4:40-4:55 Address by Guest of Honour, Kiranmai Pendyala, HR Head, AMD India
4:55-5:10 Address by Chief Guest, Padmasri N. Divakar, Chairman, Governing Body, UCE, OU
5:10-5:15 Vote of Thanks by Dr R Hemalatha, Faculty Member, ECE Dept., UCE

5:15 HIGH TEA